Amendments to the Claims

Claim 1 (currently amended): A vertical non-volatile semiconductor memory cell, comprising:

a substrate having a surface, a drain region, a channel region and a source region;

a trench formed in said substrate from said source region to said drain region, said trench formed vertically, ~~essentially~~ substantially perpendicular to said surface of said substrate, said trench having trench walls;

a first dielectric layer formed ~~essentially~~ substantially on said trench walls;

a charge storage layer for storing charges, said charge storage layer being formed on said first dielectric layer;

a control layer trench formed in said charge storage layer and defined by walls, said charge storage layer ~~surrounding~~ encircling said control layer trench;

a second dielectric layer formed at least partially on said walls of said control layer trench and having a surface;

a control layer formed ~~essentially~~ substantially on said surface of said second dielectric layer, said control layer including a control filler layer formed in a remaining part of said control layer trench and a control gate layer located on said surface of said substrate;

a trench extension formed ~~essentially~~ substantially underneath said trench, said trench extension having a surface;

a third dielectric layer formed on said surface of said trench extension; and

a filler material for at least partially filling said trench extension, said filler material separated from said control filler layer.

Claim 2 (previously amended): The vertical non-volatile semiconductor memory cell according to claim 1, wherein said filler material is electrically isolated from said charge storage layer.

Claim 3 (previously amended): The vertical non-volatile semiconductor memory cell according to claim 1, wherein said filler material is in electrical contact with said charge storage layer.

Claim 4 (previously amended): The vertical non-volatile semiconductor memory cell according to claim 1, wherein said control layer trench extends within said trench.

Claim 5 (previously amended): The vertical non-volatile semiconductor memory cell according to claim 1, wherein said control layer trench extends into said trench extension.

Claim 6 (previously amended): The vertical non-volatile semiconductor memory cell according to claim 1, wherein said control layer trench extends into said substrate beneath said trench extension.

Claim 7 (original): The vertical non-volatile semiconductor memory cell according to claim 1, wherein said first dielectric layer has a tunnel layer.

Claim 8 (original): The vertical non-volatile semiconductor memory cell according to claim 1, wherein said second dielectric layer includes an ONO layer sequence and said third dielectric layer includes an ONO layer sequence.

Claim 9 (original): The vertical non-volatile semiconductor memory cell according to claim 1, wherein said second dielectric layer has a dielectric with a high relative dielectric constant.

Claim 10 (original): The vertical non-volatile semiconductor memory cell according to claim 9, wherein said second dielectric layer has a metal oxide.

Claim 11 (original): The vertical non-volatile semiconductor memory cell according to claim 1, wherein said filler material, said charge storage layer and said control layer include a material selected from the group consisting of an electrically conductive polysilicon and a silicide.

Claim 12 (original): The vertical non-volatile semiconductor memory cell according to claim 1, wherein said control layer includes a surface layer and at least one control filler layer.

Claim 13 (original): The vertical non-volatile semiconductor memory cell according to claim 1, wherein said trench and said trench extension constitute a deep trench that is formed in a DRAM process.

Claim 14 (withdrawn): A method for manufacturing a vertical non-volatile semiconductor memory cell, which comprises:

providing a substrate;

forming a deep trench in the substrate, providing the deep trench with a third dielectric layer, and filling the deep trench with a filler material;

partially removing the filler material and the third dielectric layer in the deep trench to form an upper trench;

forming a first dielectric layer in the upper trench;

forming a charge storage layer in the upper trench;

forming a control layer trench at least partially in the charge storage layer;

forming a second dielectric layer in the control layer trench;

forming a control layer in the control layer trench; and

forming a collar isolation, a flat trench isolation and connecting elements.

Claim 15 (withdrawn): The method according to claim 14, which comprises etching the control layer trench into the upper trench.

Claim 16 (withdrawn): The method according to claim 14, which comprises etching the control layer trench into the deep trench.

Claim 17 (withdrawn): The method according to patent claim 14, which comprises etching the control layer trench into the substrate.